

The diagram shows a horizontal timeline from 0 to 4 ms. At 1 ms, a handwritten note 'TRANSITION STARTS HERE' points to the start of the signal. The 'Electronics' signal is a square wave that transitions from high to low at 1 ms. The 'LC' signal is a square wave that transitions from high to low at 1 ms. A handwritten note 'DRAW' with an arrow points to the high state of the 'Electronics' signal. A handwritten note 'BRIGHT TO DARK TRANSITION FINISHED' points to the end of the high state of the 'Electronics' signal. A handwritten note 'DARK TO BRIGHT TRANSITION FINISHED' points to the end of the low state of the 'Electronics' signal.

The diagram illustrates the timing of a pixel driver circuit. It consists of two horizontal tracks: the top track is labeled "Electronics" and the bottom track is labeled "LC".

- Electronics Track:**
 - On the far left, a vertical dashed line is labeled "INITIALIZATION OR CLEAR TIME 200".
 - Following this, a rectangular block contains a sawtooth waveform and the word "DRAW" with a right-pointing arrow.
 - After the "DRAW" block, the signal transitions to a low level.
- LC Track:**
 - The signal remains at a high level during the "DRAW" phase.
 - When the "DRAW" phase ends, the signal transitions to a low level.
 - The signal remains at the low level until the end of the frame.
- Annotations:**
 - An arrow points from the end of the "DRAW" block to the LC track, labeled "BRIGHT TO DARK TRANSITION STARTS HERE".
 - An arrow points to the start of the low-level segment on the LC track, labeled "BRIGHT TO DARK TRANSITION FINISHED".
 - An arrow points to the end of the low-level segment on the LC track, labeled "DARK TO BRIGHT TRANSITION FINISHED".
 - An arrow points to the start of the low-level segment on the LC track, labeled "DARK TO BRIGHT TRANSITION STARTS HERE".

Fig.

Fig. 2

FIG. 1B

black region 5VOLTS

white region 2.5VOLTS

black region 0VOLTS

300 310 320 330

TRANSITION ENHANCED VOLTAGE RANGE 1.5V

3.5V

FIG. 3

00010" 93602460

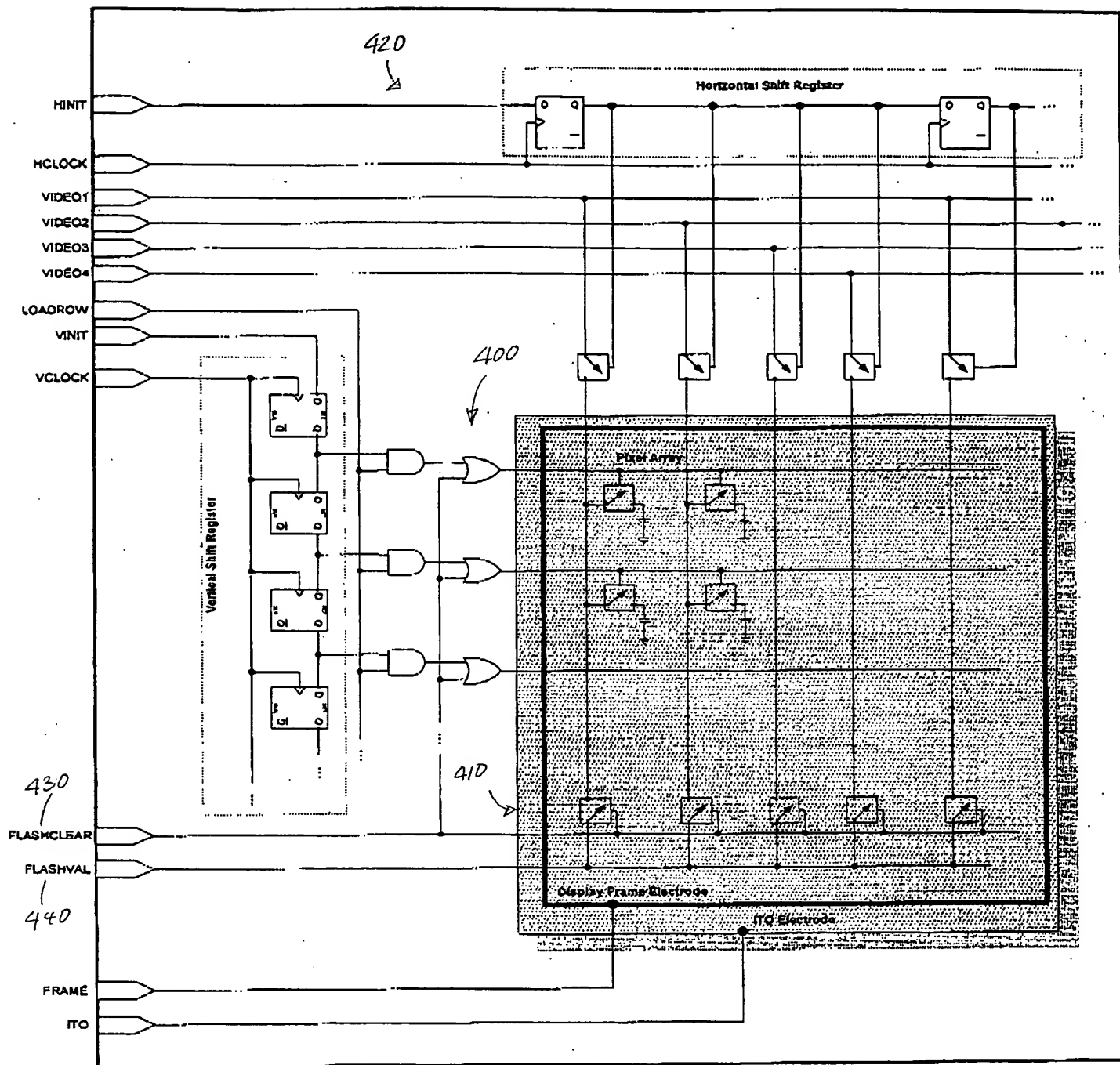
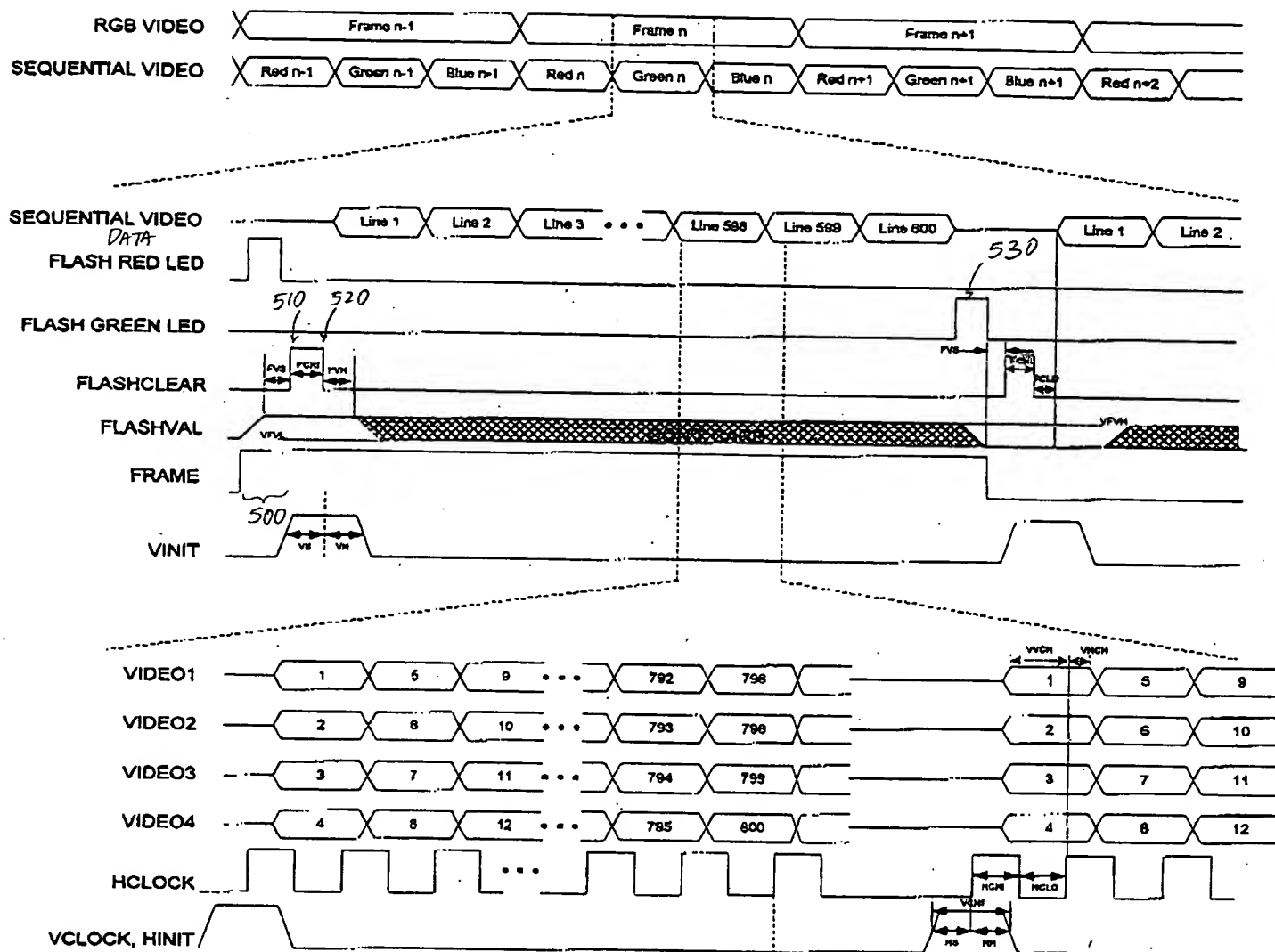


FIGURE 4



Multi-bank Mode:
SBSEL = 0, LOADROW = 1

FIGURE 5

The diagram illustrates a 4x4 matrix display driver circuit. It features a Vertical Shift Register on the left and a Horizontal Shift Register at the top. The Vertical Shift Register has four outputs, each connected to a column of four transistors in the Pixel Array. The Horizontal Shift Register has four outputs, each connected to a row of four transistors in the Pixel Array. The Pixel Array is a 4x4 grid of transistors. The Display Frame Electrode is connected to the bottom of the array, and the ITO Electrode is connected to the right side of the array. Column lines 1 and 800 are labeled.

FIG. 6

096309-0100

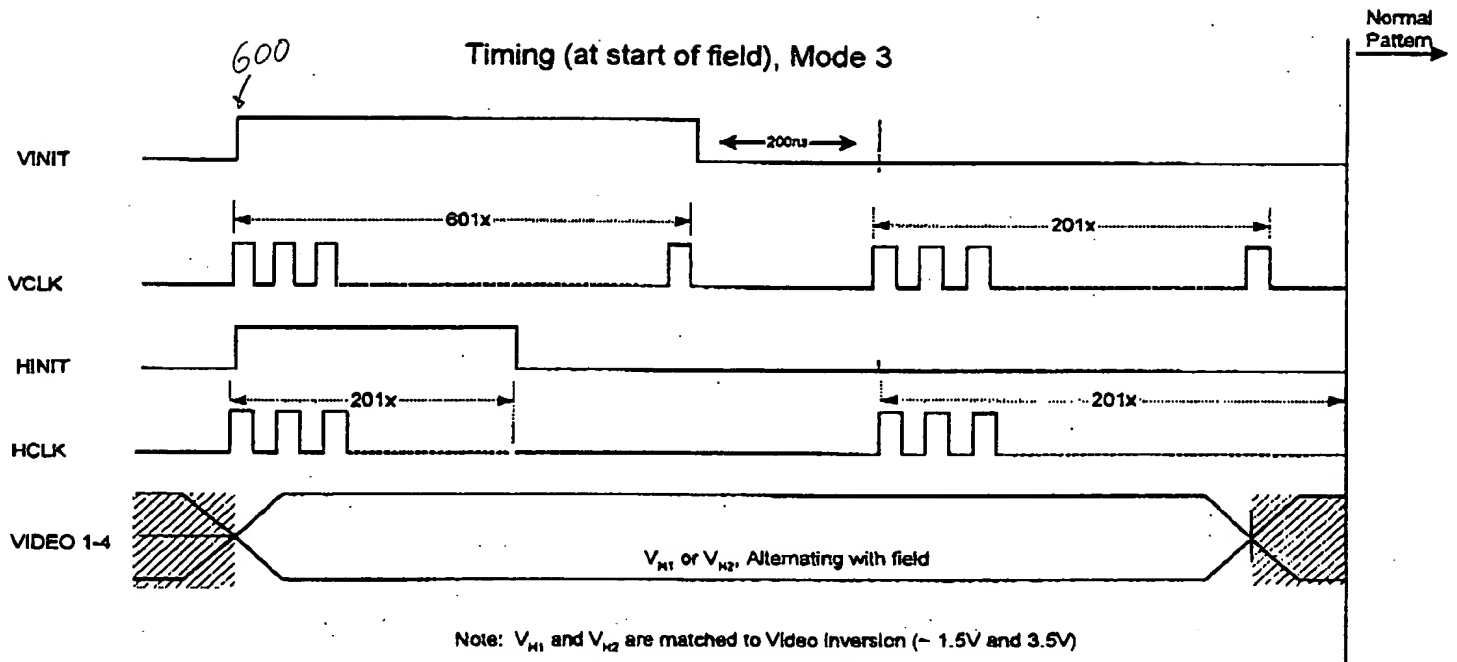


FIGURE 7